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THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP
100 GALLERIA PARKWAY, NW
STE 1750
ATLANTA, GA 30339-5948

EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,903	SHIH, PO-SHENG	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,8,13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,13 and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In an amendment dated, August 2nd, 2006, the Applicant amended claims 1-4, 7-8, 13 and 15-19 and cancelled claims 5-6, 9-12, 14 and 20-22. Currently claims 1-4, 7-8, 13 and 15-19 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4, 7-8, 13 and 15-19 have been considered but are moot in view of the new ground(s) of rejection.

3. On pages 10-13 of the amendment, the Applicant argues that there is no motivation to combine Yamamoto and Yi.

In response to Applicant's argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Yi discloses that the pixel structure and wiring scheme disclose allows for a display device that is both simple and inexpensive to manufacture. This is seen as sufficient motivation for one of ordinary skill in the art to combine the two references.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 7-8, 13 and 15-18 are rejected under 35 U.S.C. 103(a) as being anticipated by Yamamoto et al. (US 2002/0047818) in view of Yi et al. (US 6,791,522).

With respect to claim 1, Yamamoto discloses, a black image insertion method for display (para. 37), a black image (note transmittivity in the second half of a vertical scanning period) being inserted between two frames of a liquid crystal display (fig. 14), each of the frames being displayed by a plurality of liquid crystal cells (fig. 18), each of the crystal cells (C_LC in fig. 15) having a first electrode and a second electrode, the first electrode being connected to a switching transistor (TFT_S in fig. 15) and also connected to one terminal of a black image transistor (drain of TFT_C in fig. 15), a plurality of enable pulses periodically switching the switching transistor (see GL_S applied voltage pulses in fig. 14), and the second electrode being connected to a common voltage (CE in fig. 15; para. 86), the black image insertion method comprising:

sending one of the enable pulses (GL_S applied voltage pulse in fig. 14) through a scanning line to switch on the switching transistor, a voltage of the first electrode being changed to a data voltage (potential of PE in fig.14); and

sending a black image enable pulse (GL_C enable pulse in fig. 14) through a black image line to switch on the black image transistor before a next enable pulse switches on the switching transistor again, the voltage of the first electrode being changed from the data voltage to a black image voltage (the timing claimed is clear when figs. 14 and 15 are viewed together.).

Yamamoto does not expressly disclose, connecting the liquid crystal cell to the black image line, isolating the second electrode of the cell from the black image line or a common voltage that is a steady voltage value.

Yi discloses, a diode (D3 in fig. 3) connected to a reset line and an electrode (Cl in fig. 3). It is well known in the art that a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi), this is further supported by the disclosures by the Applicant (page 14, lines 24-25).

Further, Yi discloses, that the second electrode of the cell (Cl in fig. 3) is tied to ground thereby applying a steady voltage value that isolates the electrode from the reset line.

Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely LCD display pixel circuitry and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to rewire the black image transistor of Yamamoto as taught by Yi.

The motivation for doing so would have been to create a reset pixel structure that is both easier and cheaper to manufacture (Yi; col. 2, lines 1-4).

Therefore it would have been obvious to combine Yi with Yamamoto for the benefit an easier method of manufacture to obtain the invention as specified in claim 1.

With respect to claim 2, Yamamoto and Yi disclose, the black image insertion method of claim 1 (see above), wherein the black image voltage is between the common voltage plus a zero-level gray scale voltage and the common voltage minus the zero-level gray scale voltage (while Yamamoto does not expressly disclose this

limitation; as seen in the potential of PE in fig. 14 the black image voltage is equivalent to the common line voltage. Therefore it is inherent that the black image voltage of Yamamoto is between the range of the common voltage +/- a gray scale voltage, regardless of the value of the gray scale voltage.).

With respect to claim 3, Yamamoto and Yi disclose, the black image insertion method of claim 1 (see above), wherein the black image insertion method further comprises: providing an initial voltage to the black image transistor to turn off the black image transistor during sending the enable pulse to switch on the switching transistor (note the negative voltage applied during the display period in fig. 14).

With respect to claim 4, Yamamoto and Yi disclose, the black image insertion method of claim 3 (see above), wherein the black image insertion method further comprises: returning a voltage of the black image transistor to the initial voltage after the voltage of the first electrode is changed from the data voltage to the black image voltage (GL_C clearly returns to the initial voltage (2^{nd} negative initial voltage) after the element is supplied with a black voltage).

With respect to claim 7, Yamamoto discloses, the black image insertion method of claim 1 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the initial voltage and a drain of the black image transistor is connected to the first electrode, the initial voltage is lower than the data voltage and the black image enable pulse is higher than the data voltage.

Yi discloses, a diode (D3 in fig. 3) connected to a reset line and an electrode (Cl in fig. 3). As disclosed by the Applicant (page 14, lines 24-25) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi). Further, Yi discloses, that the reset diode (D3 in fig. 3) is turned on to discharge the load capacitor (col. 3, lines 9-11). This inherently requires certain voltage comparisons; namely that the initial voltage is lower than the data voltage and the black image enable pulse is higher than the data voltage.

Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely LCD display pixel circuitry and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to rewire the black image transistor of Yamamoto as taught by Yi.

The motivation for doing so would have been a both an easier and cheaper method of manufacture (Yi; col. 2, lines 1-4).

Therefore it would have been obvious to combine Yi with Yamamoto for the benefit an easier method of manufacture to obtain the invention as specified in claim 7.

With respect to claim 8, Yamamoto discloses, the black image insertion method of claim 1 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the first electrode and a drain of the black image transistor is connected to the initial voltage, the initial voltage is higher than the data voltage and the black image enable pulse is lower than the data voltage.

Yi discloses, a diode (D3 in fig. 2) connected to a reset line and an electrode (CI in fig. 2). As disclosed by the Applicant (page 18, lines 18-19) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi). Further, Yi discloses, that the reset diode (D3 in fig. 2) is turned on to discharge the load capacitor (col. 3, lines 9-11). This inherently requires certain voltage comparisons; namely that the initial voltage is lower than the data voltage and the black image enable pulse is higher than the data voltage.

For motivation and further merits of the rejection see the above rejection of claim 7.

With respect to claim 13, Yamamoto discloses, a black image insertion circuit for display, the black image insertion circuit for display comprising;

a switching transistor(TFT_S in fig. 15);

a liquid cell having a first electrode and a second electrode (C_LC in fig. 15), wherein a common voltage is constantly applied (a common voltage *is* constantly applied to the cell; the value of the common voltage applied fluctuates, not the state of applying a common voltage or not) to the second electrode (clear from fig. 14; also see para. 86);

a scan line arranged to send an enable pulse for switching the switching transistor (GL_S in fig. 15);

a data line sending pixel data to the first electrode trough the switching transistor (SL in fig. 15);

a black image electronic element (TFT_C in fig. 15), wherein the black image electronic element is connected to the first electrode (para. 86);

a black image line arranged to send a black image enable pulse for coupling with the voltage of the first electrode (GL_C in fig. 15); and

a storage capacitor connecting the first electrode and the black image line (C_STG in fig. 15); and

a black image transistor (TFT_C in fig. 15) connecting the first electrode and a common line (CL).

Yamamoto does not explicitly disclose, that the black image transistor connects the first electrode and the black image line (TFT_C in fig. 15).

Yi discloses, a diode (D3 in fig. 3) that connects a reset line and an electrode (Cl in fig. 3). It is well known in the art that a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi), this is further supported by the disclosures by the Applicant (page 14, lines 24-25).

Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely LCD display pixel circuitry and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to rewire the black image transistor of Yamamoto as taught by Yi.

The motivation for doing so would have been a both an easier and cheaper method of manufacture (Yi; col. 2, lines 1-4).

Therefore it would have been obvious to combine Yi with Yamamoto for the benefit an easier method of manufacture to obtain the invention as specified in claim 13.

With respect to claim 15, Yamamoto discloses, the black image insertion method of claim 13 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the initial voltage and a drain of the black image transistor is connected to the first electrode.

Yi discloses, a diode (D3 in fig. 3) connected to a reset line and an electrode (Cl in fig. 3). As disclosed by the Applicant (page 14, lines 24-25) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61).

Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely LCD display pixel circuitry and driving.

At the time of the invention it would have been obvious to one of ordinary skill in the art to rewire the black image transistor of Yamamoto as taught by Yi.

The motivation for doing so would have been a both an easier and cheaper method of manufacture (Yi; col. 2, lines 1-4).

Therefore it would have been obvious to combine Yi with Yamamoto for the benefit an easier method of manufacture to obtain the invention as specified in claim 15.

With respect to claim 16, Yamamoto discloses, the black image insertion method of claim 13 (see above).

Yamamoto does not expressly disclose, wherein when a source and a gate of the black image transistor are connected to the first electrode and a drain of the black image transistor is connected to the black image line.

Yi discloses, a diode (D3 in fig. 2) connected to a reset line and an electrode (CI in fig. 2). As disclosed by the Applicant (page 18, lines 18-19) a diode in this orientation is an equivalent circuit to the transistor limitations described in the current claim (also note col. 3, lines 60-61 of Yi).

For motivation and further merits of the rejection see the above rejection of claim 15.

With respect to claim 17, Yamamoto discloses, the black image insertion circuit of claim 13 (see above), wherein the black image insertion circuit further comprises a gate driver IC (110 in fig. 17), and the gate driver IC comprises:

at least one first pin connected to the scan line, the first pin is arranged to send an enable signal to switch the switching transistor (GL_S enable pulse in fig. 14); and

at least one second pin connected to the black image line, the second pin is arranged to send the black image enable pulse to the black image line (GL_C enable pulse in fig. 14), wherein a predetermined time offset exists between the enable signal and the black image enable pulse (note the time offset between the two enable pulses in fig. 14).

With respect to claim 18, Yamamoto discloses, the black image insertion circuit of claim 17 (see above), wherein periods of the enable signal and the black image enable pulse are equal (clear from fig. 14).

6. Claim 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al. (US 2002/0047818) in view of Yi et al. (US 6,791,522) and further in view of Ono et al. (US 5,526,013).

With respect to claim 19, Yamamoto and Yi disclose, the black image insertion circuit of claim 17 (see above).

Neither Yamamoto nor Yi expressly disclose, wherein periods of the enable signal and the black image enable signal are unequal.

Ono discloses, wherein periods of a reset enable pulse and a data enable pulse are unequal (col. 22, lines 43-61).

Ono, Yi and Yamamoto are analogous art because they are both from the same field of endeavor namely driving waveforms for LCD displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to alter the timing of the reset pulses of Yamamoto and Yi as taught by Ono.

The motivation for doing so would have been to lessen the degradation of the display quality (Ono; col. 2, lines 53-54).

Therefore it would have been obvious to combine Ono with Yamamoto and Yi for the benefit of a higher quality display to obtain the invention as specified in claim 19.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Asada (US 7,079,101) discloses a pixel structure comprising a diode connected transistor, see figure 25. Akimoto et al. (US 4,942,474) discloses an array of photodiodes with a diode connected transistor, in each pixel, to reset the photodiode.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
10/5/06

AMR A. AWAD
SUPERVISORY PATENT EXAMINER